

**SM2246EN Flash F/W & ISP Release Information – Q0810B**
**Introduction**

This purpose of this document is to provide release information on the SM2246EN F/W and ISP release information

**Fix Coverage**

- stands for the “new fix” or “new support” in the category
- stands for the “no-update” in the category

■ <b>Tester FW</b>	■ <b>Controller ISP</b>
<ul style="list-style-type: none"> <li>□ <b>Yield Issue</b></li> <li>■ <b>Flash Issue</b> <ul style="list-style-type: none"> <li>□ SLC Flash <ul style="list-style-type: none"> <li>□ Samsung Flash</li> <li>□ Toshiba/Sandisk Flash</li> <li>□ Intel/Micron Flash</li> <li>□ Hynix Flash</li> <li>□ Others</li> </ul> </li> <li>■ MLC Flash <ul style="list-style-type: none"> <li>■ Samsung Flash</li> <li>■ Toshiba/Sandisk Flash</li> <li>■ Intel/Micron Flash</li> <li>■ Hynix Flash</li> </ul> </li> </ul> </li> <li>□ <b>Compatibility issue</b></li> <li>□ <b>Tester Bug Fix</b></li> <li>■ <b>AP Bug Fix &amp; New Function</b></li> <li>■ <b>Feature Enhance</b></li> </ul>	<ul style="list-style-type: none"> <li>■ <b>Yield Issue</b></li> <li>■ <b>Flash Issue</b> <ul style="list-style-type: none"> <li>□ SLC Flash <ul style="list-style-type: none"> <li>□ Samsung Flash</li> <li>□ Toshiba/Sandisk Flash</li> <li>□ Intel/Micron Flash</li> <li>□ Hynix Flash</li> <li>□ Others</li> </ul> </li> <li>■ MLC Flash <ul style="list-style-type: none"> <li>■ Samsung Flash</li> <li>■ Toshiba/Sandisk Flash</li> <li>■ Intel/Micron Flash</li> <li>■ Hynix Flash</li> </ul> </li> </ul> </li> <li>□ <b>Compatibility issue</b></li> <li>■ <b>ISP Bug Fix</b></li> <li>□ <b>Feature Enhance</b></li> </ul>

**ISP Revision History**

Version	MP Tool version	ISP version	Note
Q0810B	Q0824A	Q0810B	<p>This FW supports both 2D/3D MLC NAND (does not feature SLC caching)</p> <ol style="list-style-type: none"> <li>1. Update Security Fw to version Q0727A.</li> <li>2. Update Boot ISP to version Q0609A.</li> <li>3. Support Hynix 3DV2 MLC 1CE multi-die devices.</li> <li>4. Support Samsung 14nm D-die 792 page devices.</li> <li>5. Support Samsung 1GB dram.</li> <li>6. Modify clear buffer flag algorithm in SATA error handle flow.</li> <li>7. Add pretest error code 0x2A: C_Pret_TotalFBlockOver8K and 0x2B: C_Pret_CapacityNotSupport.</li> <li>8. Set Vfr of VDT27 to 2.8V for L06B 3.3V devices.</li> <li>9. Issue Fix: FW should retrieve retry table after resuming form DEVSLP.</li> <li>10. Issue Fix: Modify the calculation for disk size reported to host. (Take TCG reserved sector count/shift count into consideration for both ISP and RDT FW)</li> <li>11. Issue Fix: Rest data in HW front-end buffer may cause the BVA halt from releasing SATA engine.</li> <li>12. Issue Fix: Sanitize frozen status should lock sanitize feature commands only.</li> <li>13. Issue Fix: HDMA count may overflow during closing part read FIFOs.</li> <li>14. Issue Fix: Apply DEVSLP after Slumber ACK Immediately would cause drive hang on DIPM Flow.</li> <li>15. Issue Fix: An error NCQ (double tag or out of range LBa ... etc) came during standby mode, FW should not return D2H in ISR.</li> <li>16. Issue Fix: For read retry sequence of Toshiba 24nm/32nm SLC NANDs, 26h command should be removed.</li> </ol>
Q0512A	Q0508A	Q0512A	<p>This FW supports both 2D/3D MLC NAND (does not feature SLC caching)</p> <ol style="list-style-type: none"> <li>1. Update security FW to version SMI_SEC_SATA_Q0330A.</li> <li>2. Update RDT FW to version: Q0512A, featuring read retry sequence for error bit count over TH.</li> <li>3. Improved early move algorithm to pass read disturb test: Butterfly Seeking.</li> </ol>

			<p>4. Add an workaround method for a host issue. Data triggering is interrupted by host power mode command.</p> <p>5. Issue fix: Incorrect dram cache size for Hynix 3DV2 from version P1225C.</p>
Q0303B	Q0321B	Q0303B	<p>This FW supports both 2D/3D MLC NAND (does not feature SLC caching)</p> <p>17. Update security FW to version SMI_SEC_SATA_Q0116A.</p> <p>18. Update BootISP to version: Q0303A.</p> <p>19. Support Samsung 14nm MLC "K9GDGD8U0B".</p> <p>20. Apply read scrub to all NANDs to prevent read disturbance.</p> <p>21. Issue Fix: For Micron L06B 2TB drive, FW reports "too much bad" without default capacity setting during pretest flow.</p> <p>22. Issue Fix: As program fail handle is disabled, minimum size of cache buffer(for host data) should be 3.5*size of super page, to prevent dram buffer flag issue.</p> <p>23. Issue Fix: FW may refer to bit 0 of status register to check cache status.</p> <p>24. Issue Fix: During sata error handle sequence, HW BVA reset may stop HDMA data transfer.</p> <p>25. Issue Fix: Check HW command queue done before applying set feature sequence to NAND flash.</p>
P1225C	Q0113B	P1225C	<p>This FW supports both 2D/3D MLC NAND (does not feature SLC caching)</p> <p>26. Support Micron L06B 2TB capacity.</p> <p>27. Reduce command latency as GC is under operation.</p> <p>28. Add one check spare seed mode to detect any plane "ALL FFh" pattern output. (in check EOB of Tail block or build F2H Map for unfull block)</p> <p>29. Avoid specific L06B Train ADJ Fail in MP Flow. (Bit flip of parity of spare data)</p> <p>30. Add vendor unique command for VPX to perform external destroy.</p> <p>31. Add customized erase unit function for VPX.</p> <p>32. Add MP option, if RDT Fail, keep ALL block program state, Don't Erase. (UFD Sorting)</p> <p>33. Issue fix: As program fail handle is disabled, minimum size of cache buffer(for host data) should be 3*size of super page, to prevent dram buffer flag issue.</p> <p>34. Issue Fix: Modify the cases that FW would clear</p>

			<p>following commands as LSCS occurs.</p> <p>35. Issue Fix: As enable/disable write cache is set by SCT command, the feature can not be changed by set feature command. Device should not return error as well.</p> <p>36. Issue Fix: Initialize Link Table Info entirely in Erase Unit, in case that misplaced Link Table Info might be saved afterward.</p> <p>37. Issue Fix: Save security info prior to Prepare Fast Boot procedure before entering DEVSLP to keep fast boot ID for Link Block.</p> <p>38. Issue Fix: Variable overload leads to FW return wrong status.</p>
P1111A	P1125A	P1111A	<p>This FW supports both 2D/3D MLC NAND (no SLC caching)</p> <p>1. Update SecurityFW to version: SMI_SEC_SATA_P1027A.</p> <p>2. Update RDT to version P1027RDT: Modify that FW would output all FFh pattern in MP "Self Test Result" list for L06B 512GB and 1TB capacity.</p> <p>3. Support 65h command to switch internal die for some specific NANDs.</p> <p>4. For different type of SanDisk 1znm NAND, corresponding retry table is supported.</p> <p>5. Improve cache program performance.</p> <p>6. During power on flow, make spare blocks with minimum P/E count being used first.</p> <p>7. Check spare seed for WPRO and Link block to prevent the case: all FFh pattern output by any plane.</p> <p>8. Add pretest error code 0x28: CannotFindSysBlk to indicate number of bad block in each slot.</p> <p>9. Issue fix: As SM2246EN force write cache is enabled, FW should not return error status as host apply disable write cache.</p>
P1003B	P1018B	P1003B	<p>This FW supports both 2D/3D MLC NAND (no SLC caching)</p> <p>39. Update Security API</p> <p>40. Reduce time consumption on dram access in update/check map functions.</p> <p>41. Return COMRESET status in ISR if COMRESET occurs in Trim.</p> <p>42. Return previous one SAMRT data as latest WPRO page is UECC.</p> <p>43. Add pretest error code: 0x29 to sort power-on one pass L06B.</p>

			<ul style="list-style-type: none"> <li>44. Add max/min Temp. in SMART ID: 0xC2(optional setting in MP tool).</li> <li>45. Add flush dram as SPOR feature for 3.3V devices.</li> <li>46. Fix the issue that FW may not enable HW interrupt if power drops(VDT40 and VDT27) and recover then.</li> <li>47. Fix the issue that writing same data is seen as UNC during ATA command: SMART EXECUTE OFFLINE IMMEDIATE(0xD4).</li> </ul>
P0614D	P0628B	P0614D	<p>This FW supports both 2D/3D MLC NAND (no SLC caching)</p> <ul style="list-style-type: none"> <li>1. Update Security FW to SMI_SEC_SATA_P0701A.</li> <li>2. Update RDT FW version to P0614RDT.</li> <li>3. Update Boot ISP version to P0801A: For Intel L06B single plane read may cause ECC fail under a specific condition.</li> <li>4. Add NAND sorting for SM3259.</li> <li>5. Add Lower Page Protection (LPP) for I/M L06B 3.3V devices.</li> <li>6. Pass WHCK-EHDD TPerReset test case on Windows 10.</li> <li>7. Pass WHCK-EHDD RangeCrossing test case on Windows 10.</li> <li>8. Abort FW Update operation, if the Security Settings don't remain the same.</li> <li>9. Fix issue: CRYPTO SCRAMBLE EXT command can't be successfully implemented when only AES is enabled.</li> </ul>
P0614B	P0624A	P0614B	<ul style="list-style-type: none"> <li>1. This FW supports both 2D/3D MLC NAND</li> <li>2. Enable "ODT by controller" for IM L06B 1TB drive.</li> <li>3. Modify strong/weak page table #04.</li> <li>4. Improve sequential read performance for 4-plane 16K-page devices.</li> <li>5. Support new form factor: CFast.</li> <li>6. Fix the issue of NCQ soft reset, where host could not send out FIS H2D.</li> <li>7. Fix the issue: During map saving, the last saved tail block should be empty block as its valid page count is 0.</li> <li>8. Fix the issue: During getting page pointer of data block, command queue may hang under corner case as program fail handle is disabled.</li> <li>9. Fix the issue: After moving WPRO block, meta data of plane 1 may be incorrect.</li> <li>10. Add the mechanism that block 0 is included in check system block flow during pretest flow.</li> <li>11. Fix the issue: Dummy pages of EOB may be filled with wrong serial.</li> </ul>
O1225L	P0526A	O1225L	<ul style="list-style-type: none"> <li>1. Support Mira dram (256MB/512MB)</li> <li>2. Modify save map policy: limit partial save map time</li> </ul>

			<p>consumption</p> <ol style="list-style-type: none"> <li>3. Modify issue of SSD cannot boot to Win8.1 when SATA Gen2 is forced</li> <li>4. Add new pretest error code 0x26: Run time/RDT too much bad</li> <li>5. Add backup page for erase unit info in WPRO block</li> <li>6. Improve sequential read performance for 4-plane 16K-page flash (including Toshiba/SanDisk 15nm).</li> <li>7. Modify strong/weak page table.</li> <li>8. Fix NCQ soft reset issue, where host could not send out FIS H2D.</li> <li>9. Fix issue of during the process of saving map, last saved tail block should be empty block as its valid page count is 0.</li> <li>10. Fix issue of during the process of getting page ID of data block, command queue may hang under corner case as program fail handling is disabled.</li> <li>11. Fix issue of after moving WPRO block, meta data of plane 1 may be incorrect.</li> </ol>
O1225J	P0412B	O1225J	<ol style="list-style-type: none"> <li>1. MP tool P0412B cannot swap ISP without being with ISP O1225J. Please don't use other version of ISP to be with MP tool P0412B to swap ISP.</li> <li>2. 3D MLC is not supported by this FW</li> <li>3. Modify features of thermal throttling.</li> <li>4. Modify partial cleaning mechanism to avoid large time-consuming on loading EOB</li> <li>5. Add an extra read method to handle NCQ read commands.</li> </ol>
P0115G	P0223B	P0115G	<ol style="list-style-type: none"> <li>1. Support Hynix 3D V2 MLC (SSD 128/256GB)</li> <li>2. Support Micron L06B (SSD 128/256GB)</li> <li>3. Support new seed table (1024 sets)</li> <li>4. Extend table corresponding to physical page (strong page/weak page) to 2KB</li> <li>5. Modify RDT for Micron L06B</li> <li>6. Fix the issue of loading code when the SSD is recovered from DEVSLP</li> </ol>
O1225G	P0219B	O1225G	<ol style="list-style-type: none"> <li>1. Modify that if "erase operation" was interrupted in the last power-on, return status to host and open HDRS interrupt before continuing doing erase operation.</li> <li>2. Record LUN number in RDT test fail information and show in MP tool self test result.</li> <li>3. Add an option, TotalFailCntTH, for the number of RDT Fail Threshold</li> <li>4. Abort R/W commands when the address which would be accessed beyond the range can be supported by drive (case of over flow is detected)</li> <li>5. Ram test flow is modified for higher coverage</li> <li>6. Use "compared seed" to detect all 0xFF read data during read</li> </ol>

			<p>retry sequence</p> <ol style="list-style-type: none"> <li>7. Modify read log extend command "Log address 04h-Device Statistics", in which Logical Sectors Written/ Number of Write Commands/ Logical Sectors Read/ Number of Read Commands should be recorded in 48 bits</li> <li>8. Modify the key management that each range has different key in the first place</li> <li>9. Modify Program Fail Read Back Algorithm</li> <li>10. Restore divided crystal frequency in shutdown process of DEVSLP function</li> </ol>
O1225E	P0114A	O1225E	<ol style="list-style-type: none"> <li>1. Doesn't support AES/security related function.</li> <li>2. Modify that if "erase operation" was interrupted in the last power-on, return status to host and open HDRS interrupt before continuing doing erase operation.</li> <li>3. Record LUN number in RDT test fail information and show in MP tool self test result.</li> <li>4. Add an option, TotalFailCntTH, for the number of RDT Fail Threshold</li> <li>5. Abort R/W commands when the address which would be accessed beyond the range can be supported by drive (case of over flow is detected)</li> <li>6. Ram test flow is modified for higher coverage</li> <li>7. Use "compared seed" to detect all 0xFF read data during read retry sequence</li> <li>8. Modify read log extend command "Log address 04h-Device Statistics", in which Logical Sectors Written/ Number of Write Commands/ Logical Sectors Read/ Number of Read Commands should be recorded in 48 bits</li> <li>9. Modify the key management that each range has different key in the first place</li> <li>10. Modify Program Fail Read Back Algorithm</li> </ol>
O1026A	O1027A	O1026A	<ol style="list-style-type: none"> <li>1. Modify crystal frequency in order to avoid it's too low to latch signals from SATA interface during the resume process.</li> <li>2. Modify system PLL in case that the controller will encounter power-loss which is caused by sudden high peak frequency.</li> <li>3. Modify the flow of SMART and security if UGSD occurs when doing "erase operation"</li> <li>4. Add read back mechanism to check the authentication of program fail in RDT for SanDisk 1znm.</li> <li>5. Add one mechanism to save event log</li> </ol>
O0918B	O0910A	O0918B	<ol style="list-style-type: none"> <li>1. Modify read retry sequence for Hynix 16nm B-Die</li> <li>2. Add bitmap scrub operations for SanDisk 1znm</li> </ol>

			<ol style="list-style-type: none"> <li>Support single 1GB DRAM (Vendor: Micron)</li> <li>Fix the issue for power cycling during erase map info block</li> </ol>
O0821D	O0819A	O0821D	<ol style="list-style-type: none"> <li>Support SID Authority Disable Proposal – Microsoft</li> <li>Support Mandatory GUIDID Proposal - Microsoft</li> <li>Support Geometry Reporting Feature – Alignment</li> <li>For Hynix 20nm B die flash, fix the bug of flash ID changing after issuing “set feature”.</li> <li>Fix ATA security bug when AES is disabled</li> <li>Fix the issue of internal interleave</li> </ol>
O0724B	O0722C	O0724B	<ol style="list-style-type: none"> <li>Support Toshiba 24nm SLC</li> <li>Support SanDisk 24nm MLC</li> <li>Support SanDisk A19 (1Y) MLC</li> <li>Modify program fail handling procedure</li> <li>Support Toshiba 15nm SLC mode (A2 command)</li> <li>Change Tper authentication to “Anybody authority”</li> <li>Support IEEE 1667 CONFIGURE SILOS command</li> </ol>
O0617A	O0618A	O0617A	<ol style="list-style-type: none"> <li>This FW can support security and non-security FW that are corresponding to SM2246EN_AB and SM2246EN_AA.</li> <li>MP will detect the controller automatically. If the controller is SM2246AA, MP will block security related functions. If the controller is SM2246AB, MP will show the options of security related functions.</li> <li>Fix the issue related to read command access interface of TCG.</li> <li>Make sure that the related hardware settings constrained to change AES keys are fully performed.</li> <li>Fix the bug that when issuing. SMART_EXECUTE_OFFLINE_IMMEDIATE command which may cause the FW not be able to enter low-power mode.</li> <li>Make sure that partial / slumber mode can be low-power.</li> <li>Capacity of SSD would not be influenced when supporting TCG function.</li> </ol>
N1126K	O0522A	N1126K	<ol style="list-style-type: none"> <li>Modified SMART attribute reset: ID 0xA4~0xA7, 0xAF, 0xC7 and 0xF5</li> <li>Returned status would include <ul style="list-style-type: none"> <li>Pure spare count if the threshold is not exceeded</li> </ul> </li> </ol>



			<ul style="list-style-type: none"> <li>● Erase count if the threshold is exceeded</li> </ul> <ol style="list-style-type: none"> <li>Fixed trim bug: when LBA of trim command is higher than total LBA, this command should be returned</li> <li>Turn LED off when trim command is processed</li> <li>Solved device sleep DRAM backup issue: flash retry FIFO should not be overlapped by DRAM data</li> <li>Solved spare block run out issue: successive Map block can be used</li> </ol>
N1126F	O0327A	N1126F	<ol style="list-style-type: none"> <li>Fix overflow issue of read – retry table that Hynix NAND flash use.</li> <li>Fix U-link NCQ-03 script issue</li> <li>Support Sandisk 1znm flash.</li> <li>Support Hynix 16nm F-die flash.</li> <li>Add CID options for enabling DRAM SRT feature.</li> </ol>
N1114H	N1114A	N1114H	<ol style="list-style-type: none"> <li>Fix DEVSLP issue</li> <li>Fix time-out issue of downloading microcode.</li> </ol>
N1114B	N1114A	N1114B	<ol style="list-style-type: none"> <li>Support 4Die/1CE Flash</li> <li>Support new VU command for Serial Number change</li> <li>Support disk self-destroy function (erase all disk data via GPIO)</li> <li>Extend # of bad block combination to 2048 to improve 1TB initialization</li> <li>Modify Pretest Bad Block Threshold as configurable from 0 to 255</li> <li>Bug fix of Trim command and potential command timeout/abort.</li> <li>Support Samsung K9QDGD8U5M</li> </ol>
N1007C	N0918A	N1007C	<ol style="list-style-type: none"> <li>Support TSB 15nm MLC.</li> <li>Support of Sanitize (erase all block feature).</li> <li>Improve command response time with background map rebuild.</li> <li>Improve Macbook installation compatibility.</li> <li>Improve Pretest flow in the cases of reference original and runtime bad.</li> <li>Enhance error/event log structure and content.</li> <li>Enable CDI interrupt iff DEVSLP had been configured and enabled by CID and host.</li> <li>Resolve bugs/issues of NCQ read flow, Flash setting at DEVSLP resume, Trim command handling, program fail handling in swapping active block.</li> </ol>
N0815B	N0815A	N0815B	<ol style="list-style-type: none"> <li>Fix of program fail handling on pure SLC Flash.</li> <li>Improvement to resolve read disturbance on Hynix 16nm</li> </ol>

			<p>MLC Flash.</p> <ol style="list-style-type: none"> <li>Improvement to speed up boot time by storing WPRO page index information.</li> <li>Bug fix of program fail.</li> <li>Fix of SPOR timeout issue on 512GB/1TB disk.</li> <li>Bug fix of LTS and RDT.</li> <li>Bug fix of pretest failure on Samsung 21nm Flash.</li> <li>Improvement of random read performance in internal interleave mode.</li> <li>Support of full disk SLC mode on Micron Flash.</li> </ol>
N0711A	N0704B	N0711A	<ol style="list-style-type: none"> <li>Fix cache program bug since N0704A.</li> <li>Fix program fail handle bug for internal interleave mode since N0704A</li> <li>Fix an IPM issue since FW N0516D which automatically change Partial to Slumber in HIPM if DIPM was enabled.</li> <li>Extend bad block combination number from 512 to 1024.</li> <li>Decide Hynix read-retry count by using OPT command instead of predefine value from MP package.</li> <li>Support Internal Interleave.</li> <li>Support program fail handling</li> <li>Modify trim flow for the performance with Marvell RAID chip</li> <li>Support Hynix 16nm 64Gb MLC: H27QCG8T2E5R, H27QEG8VEE5R</li> <li>Support Hynix 16nm 128Gb MLC: H27QEG8UDB8R, H27QFG8VEB8R-BCF, H27Q1T8YEB9R (CS sample and after )</li> </ol>
N0530C	N0529A	N0530C	<ol style="list-style-type: none"> <li>ISP Bug fix: Erase count miss-match after doing security erase</li> <li>Pretest Bug fix: Load L85A reclaim flash original bad bug found in N0530A</li> <li>Fix an IPM issue since FWN0516D, which cannot enter IPM mode normally.</li> </ol>
N0530A	N0529A	N0530A	<ol style="list-style-type: none"> <li>Support auto partial to slumber in HIPM</li> </ol>

			<ol style="list-style-type: none"> <li>Fill up the active block's valid pages word line when receiving Standby Immediately and swapping active block after power on</li> <li>Save SMART attribute every 20 minutes</li> <li>Save SMART info when receiving Standby Immediately</li> <li>Fine tune a read cache judgment</li> </ol>
N0402C	N0415A	N0402C	<ol style="list-style-type: none"> <li>Support 4CH8WAY interleave for 512page/block flash (L85A/L95B)</li> <li>Support 1TB capacity</li> <li>Fix DEVSLP bugs</li> <li>Support the entrance of device sleep without slumber mode first. (CID 0x4D.bit7)</li> <li>Fix the bug of occasional ISP hangs-up if power off while security erase</li> <li>Fix the bug of building the wrong mapping table after resuming from device sleep</li> <li>RDT update: Show the wrong fail message at MP result window</li> <li>Update L95B ECC to 60b in database</li> </ol>
N0307A	N0307A	N0307A	<ol style="list-style-type: none"> <li>Speed up boot up time by saving spare bitmap table, and shortening mapping table reset time.</li> <li>Re-issue flash multi-plane ALE after disabling read-retry.</li> <li>Issue one plane ALE instead of multi-plane in read-retry.</li> <li>Extend the ALE, CLE and write pulse width when setting read-retry sequence in EDO mode.</li> <li>Enable hardware write protect.(GPIO p1.bit1)</li> <li>Enable quick erase.(GPIO P1.bit5)</li> <li>Fix the SMART value (attribute ID 0x05) miss-match issue</li> <li>Fix a markbad bug. (N0227A issue from VCT)</li> <li>Fix SMART info miss match issue.</li> <li>Fix read and write log DMA extend command bug.</li> <li>Fix RDT firmware cannot recognize MP vendor command issue.</li> </ol>

			12. Support 16k 4plane flash.
N0103B	N0114A	N0103B	<ol style="list-style-type: none"> <li>1. Fix the bug of issuing Samsung 19nm read try command by EDO mode</li> <li>2. Support DMA read log extend and DMA write log extend.</li> <li>3. Support DMA read buffer and DMA write buffer.</li> <li>4. Mark bad block by single block instead of super block and use rest good block to re-combine super block.</li> <li>5. Support DMA download microcode</li> <li>6. Add full dram size test in pretest</li> </ol>
M1213C	M1226A	M1213C	<ol style="list-style-type: none"> <li>1. Support Micron/Intel L85A, L84C,</li> <li>2. Support Micron/Intel L95B</li> <li>3. Support Samsung 19nm MLC</li> <li>4. Fix seek &amp; read verify sector command bug</li> <li>5. Support PIO Multiple mode to 2</li> <li>6. Fix SCT write same bug</li> <li>7. Enhance SPOR protection</li> <li>8. Write performance enhancement</li> <li>9. Fix a FW bug of WHCK Trim test</li> <li>10. Reduce DEVSLP power consumption</li> <li>11. Fix a read try bug for Micron/Intel NAND</li> <li>12. Support Download Micro Code</li> </ol>
M1024C	M1024A	M1024C	<ol style="list-style-type: none"> <li>1. Fix ATACT seek &amp; read verify sector command bug.</li> <li>2. Fix the error of scaling down the number of interleave</li> <li>3. Add QC tool functions</li> </ol>
M1011A	M1009B	M1011A	<ol style="list-style-type: none"> <li>1. Enhance ATA command support for Ulink test</li> <li>2. Disable all flash CE if channel is idle.</li> <li>3. Fix a power-cycling bug</li> <li>4. Fix SN number issue when KeepSN is not 20 byte length.</li> </ol>
M1003B	M1003A	M1003B	<ol style="list-style-type: none"> <li>1. Fix IM20nm read retry bug and add more options for read retry. Issue flash reset command before retry sequence.</li> <li>2. Fix build-link bug in 4ch8way</li> </ol>

			<ol style="list-style-type: none"> <li>Fix SPOR function bugs</li> <li>Disable dram compensation</li> <li>Lower schmitt trigger windows)</li> <li>Fix seek, read verify sector, and RW multiple command bug</li> <li>Fix a wear leveling bug</li> <li>Support Few Samsung &amp; Hynix dram.</li> <li>Support LTS and fix bugs of RDT function. Add the loop option in RDT</li> <li>Add Micron20nm SLC read-retry table.</li> <li>Add Dram 380Mhz option.</li> <li>Enable write cache as a default.</li> <li>Modify dram VDT from 1.4 to 1.3v.</li> </ol>
M0808A	M0808B	M0808A	<ol style="list-style-type: none"> <li>Fix Toshiba &amp; Sandisk flash read-retry error.</li> <li>Enhance SATA error handling</li> <li>Switch to dummy write if the number of spare block decreases to zero, and do not mark bad block</li> <li>Modify SMART command for WAF</li> <li>Extend the number of write log page to 32</li> <li>Fix strong page size bug on M0719</li> <li>Fix pretest bug for manual toggle flash.</li> <li>Add RDT function.</li> <li>Don't reset DRAM when resume</li> </ol>
M0719A	M0716B	M0719A	<ol style="list-style-type: none"> <li>Support Samsung 21nm K9GCG MLC</li> <li>Support Toshiba 19nm 16KB 2Plane MLC</li> <li>Support Hynix H27QCGDT2BLR, H27QEGDVEBLR</li> <li>Support Micron L84A Onfi MLC</li> <li>Support Micron L85A Onfi MLC</li> </ol>

**Note:**

- F/W and ISP update is recommended.
- History # is denoted by "Version-Date" .

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